LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A content addressable memory (CAM) system comprising:

at least one CAM entry comprising a plurality of CAM fields, the plurality of CAM fields comprising a first field and a second field, the first field being associated with a physical address and the second field being associated with a virtual address;

at least one input selector that enables access to the first field in a first mode and the second field in a second mode; and

a match evaluator that compares the enabled ~~fields~~ field to a search value.

2. (Cancelled)

3. (Previously Presented) The system of claim 1, at least one of the first field and the second field is interleaved with at least one other of the plurality of CAM fields.

4. (Original) The system of claim 1, the match evaluator comprising at least one pull-down field effect transistor.

5. (Original) The system of claim 1, the at least one input selector comprising at least one multiplexer.

6. (Original) The system of claim 1, further comprising a driver that provides a control input to the input selector and provides a given search value to the match evaluator.

7. (Original) A memory cache system comprising the system of claim 1.

8. (Original) A processor assembly comprising the memory cache system of claim 7.

9-15 (Cancelled)

16. (Original) A method for selecting a search mode associated with a content addressable memory system (CAM), the method comprising:

selecting between a virtual address mode and a physical address mode;

enabling access to a stored physical address associated with the CAM if the physical address mode is selected;

enabling access to a stored virtual address associated with the CAM if the virtual address mode is selected; and

comparing the enabled address to a search value.

17. (Original) The method of claim 16, the selecting comprising configuring a plurality of multiplexers with a common enable signal to one of a virtual address mode and a physical address mode.

18. (Original) The method of claim 16, the comparing of the enabled address to a search value comprising driving a pull-down field effect transistor (FET) with an exclusive-OR (XOR) gate receiving respective bits of the enabled address and the search value.

19. (Currently Amended) A method of searching a content addressable memory (CAM) comprising:

selecting a first CAM field from a memory entry in a first mode and a second CAM field from the memory entry in a second mode, the first CAM field comprising one of a virtual address and a physical address and the second CAM field comprising the other of the virtual address and the physical address; and

enabling access between comparison logic associated with the CAM and the selected one of the first CAM field and the second CAM field.

20. (Cancelled)

21. (Previously Presented) The method of claim 19, the selecting one of the first CAM field and the second CAM field comprising providing a control signal that has a first state in the first mode and a second state in the second mode to one or more input selectors.

22. (Currently Amended) A system for searching a content accessible memory (CAM), comprising:

means for selectively enabling access to a stored physical address associated with a first CAM field if a physical address mode is selected and a stored virtual address associated with a second CAM field if a virtual address mode is selected; and

means for comparing the selectively enabled CAM field to a search value.

23. (Previously Presented) The system of claim 22, further comprising means for providing a control signal to the means for selectively enabling, the control signal having a first state in the physical address mode and a second state in a virtual address mode.

24. (Previously Presented) The system of claim 22, the CAM system being a translation look-aside buffer.

25. (Previously Presented) The system of claim 1, the CAM system being a translation look-aside buffer.

26. (Previously Presented) The system of claim 1, wherein the CAM entry comprises a plurality of storage units, at least one of the plurality of storage units being associated with both the first field and the second field.

27. (Previously Presented) The method of claim 16, the CAM system being a translation look-aside buffer.

28. (Previously Presented) The method of claim 19, the CAM system being a translation look-aside buffer.

29. (Previously Presented) The method of claim 19, further comprising interleaving the first CAM field in the memory entry with the second CAM field in the memory entry.

30. (Previously Presented) The method of claim 19, wherein each memory entry comprises a plurality of storage units, at least one of the plurality of storage units being associated with both the first CAM field and the second CAM field.